# 128Mbyte (32Mx32) 72-pin Fast Page Mode 4K Ref. SIMM Design 5V
## Part No. HMD32M32M16G

## GENERAL DESCRIPTION

The HMD32M32M16G is a 32M x 32bit dynamic RAM high-density memory module. The module consists of sixteen CMOS 16M x 4bit DRAMs in 32-pin TSOPII packages mounted on a 72-pin, double-sided, FR-4-printed circuit board. A 0.1uF decoupling capacitor is mounted on the printed circuit board for each DRAM components. The module is a Single In-line Memory Module with edge connections and is intended for mounting in to 72-pin edge connector sockets. All module components may be powered from a single 5V DC power supply and all inputs and outputs are TTL-compatible.

## FEATURES

**w**Part Identification
HMD32M32M16G-- 4K Cycles/64ms Ref. Gold

**w** Access times : 50, 60ns
**w** High-density 128MByte design
**w** Single + 5V ±0.5V power supply
**w** JEDEC standard pinout
**w** Fast Page mode operation
**w** TTL compatible inputs and outputs
**w** FR4-PCB design

## OPTIONS MARKING

**w** Timing
50ns access -5
60ns access -6

**w** Packages
72-pin SIMM M

## PERFORMANCE RANGE

| SPEED | tRAC | tCAC | tRC |
|---|---|---|---|
| -5 | 50ns | 13ns | 90ns |
| -6 | 60ns | 15ns | 110ns |

## PRESENCE DETECT PINS

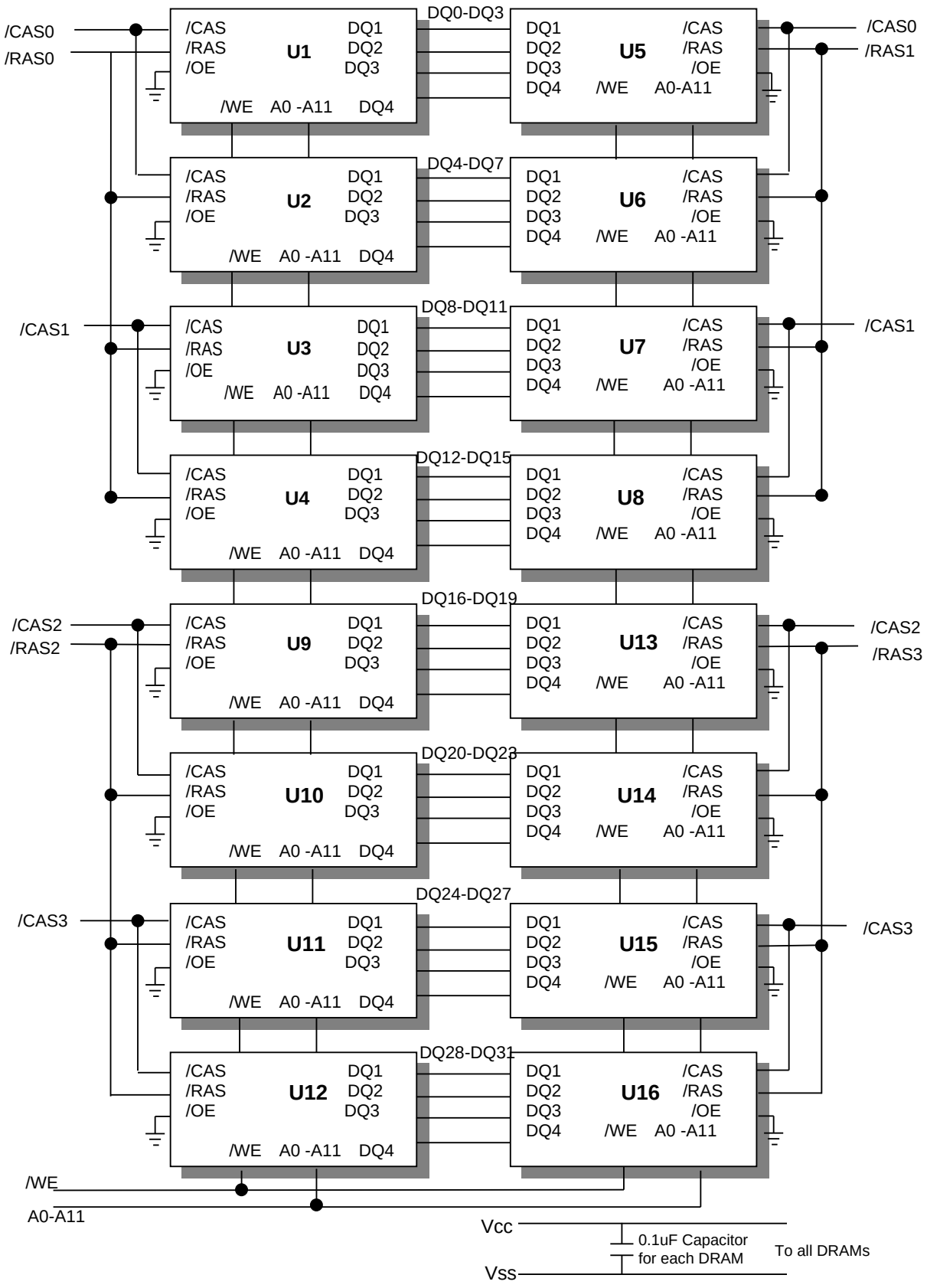
| Pin | 50ns | 60ns |
|---|---|---|
| PD1 | NC | NC |
| PD2 | Vss | Vss |
| PD3 | Vss | NC |
| PD4 | Vss | NC |

## PIN ASSIGNMENT

| PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL |
|---|---|---|---|---|---|
| 1 | Vss | 25 | DQ22 | 49 | DQ8 |
| 2 | DQ0 | 26 | DQ7 | 50 | DQ24 |
| 3 | DQ16 | 27 | DQ23 | 51 | DQ9 |
| 4 | DQ1 | 28 | A7 | 52 | DQ25 |
| 5 | DQ17 | 29 | A11 | 53 | DQ10 |
| 6 | DQ2 | 30 | Vcc | 54 | DQ26 |
| 7 | DQ18 | 31 | A8 | 55 | DQ11 |
| 8 | DQ3 | 32 | A9 | 56 | DQ27 |
| 9 | DQ19 | 33 | /RAS3 | 57 | DQ12 |
| 10 | Vcc | 34 | /RAS2 | 58 | DQ28 |
| 11 | NC | 35 | NC | 59 | Vcc |
| 12 | A0 | 36 | NC | 60 | DQ29 |
| 13 | A1 | 37 | NC | 61 | DQ13 |
| 14 | A2 | 38 | NC | 62 | DQ30 |
| 15 | A3 | 39 | Vss | 63 | DQ14 |
| 16 | A4 | 40 | /CAS0 | 64 | DQ31 |
| 17 | A5 | 41 | /CAS2 | 65 | DQ15 |
| 18 | A6 | 42 | /CAS3 | 66 | NC |
| 19 | A10 | 43 | /CAS1 | 67 | PD1 |
| 20 | DQ4 | 44 | /RAS0 | 68 | PD2 |
| 21 | DQ20 | 45 | /RAS1 | 69 | PD3 |
| 22 | DQ5 | 46 | NC | 70 | PD4 |
| 23 | DQ21 | 47 | /WE | 71 | NC |
| 24 | DQ6 | 48 | NC | 72 | Vss |

**72 PIN SIMM TOP VIEW**

## FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATING |
|---|---|---|
| Voltage on Any Pin Relative to Vss | $V_{IN ,OUT}$ | -1V to 7.0V |
| Voltage on Vcc Supply Relative to Vss | Vcc | -1V to 7.0V |
| Power Dissipation | $P_D$ | 16W |
| Storage Temperature | $T_{STG}$ | -55°C to 150°C |
| Short Circuit Output Current | $I_{OS}$ | 50mA |

w Permanent device damage may occur if " Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED DC OPERATING CONDITIONS

( Voltage reference to $V_{SS}$, $T_A$=0 to 70 °C )

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage | Vcc | 4.5 | 5.0 | 5.5 | V |
| Ground | Vss | 0 | 0 | 0 | V |
| Input High Voltage | $V_{IH}$ | 2.4 | - | Vcc+1 | V |
| Input Low Voltage | $V_{IL}$ | -1.0 | - | 0.8 | V |

## DC AND OPERATING CHARACTERISTICS

| SYMBOL | SPEED | MIN | MAX | UNITS |
|---|---|---|---|---|
| $I_{CC1}$ | -5 | - | 1920 | mA |
| | -6 | - | 1760 | mA |
| $I_{CC2}$ | Don't care | - | 32 | mA |
| $I_{CC3}$ | -5 | - | 1920 | mA |
| | -6 | - | 1760 | mA |
| $I_{CC4}$ | -5 | - | 1120 | mA |
| | -6 | - | 960 | mA |
| $I_{CC5}$ | Don't care | - | 16 | mA |
| $I_{CC6}$ | -5 | - | 1920 | mA |
| | -6 | - | 1760 | mA |
| $I_{I(L)}$ | | -10 | 10 | µA |
| $I_{O(L)}$ | | -5 | 5 | µA |
| $V_{OH}$ | | 2.4 | - | V |
| $V_{OL}$ | | - | 0.4 | V |

$I_{CC1}$ : Operating Current * (/RAS , /CAS , Address cycling @$t_{RC}$=min.)

$I_{CC2}$ : Standby Current ( /RAS=/CAS=$V_{IH}$ )

$I_{CC3}$ : /RAS Only Refresh Current * ( /CAS=$V_{IH}$, /RAS, Address cycling @$t_{RC}$=min )

$I_{CC4}$ : Fast Page Mode Current * (/RAS=$V_{IL}$, /CAS, Address cycling @$t_{PC}$=min )

$I_{CC5}$ : Standby Current (/RAS=/CAS=Vcc-0.2V )

$I_{CC6}$ : /CAS-Before-/RAS Refresh Current * (/RAS and /CAS cycling @$t_{RC}$=min )

$I_{IL}$ : Input Leakage Current (Any input 0V ≤ $V_{IN}$ ≤ 6.5V, all other pins not under test = 0V)

$I_{OL}$ : Output Leakage Current (Data out is disabled, 0V ≤ $V_{OUT}$ ≤ 5.5V

$V_{OH}$ : Output High Voltage Level ($I_{OH}$= -5mA )

$V_{OL}$ : Output Low Voltage Level ($I_{OL}$ = 4.2mA )

* NOTE: $I_{CC1}$, $I_{CC3}$, $I_{CC4}$ and $I_{CC6}$ are dependent on output loading and cycle rates. Specified values are obtained with the output open. $I_{CC}$ is specified as an average current. In $I_{CC1}$ and $I_{CC3}$, address cad be changed maximum once while /RAS=$V_{IL}$. In $I_{CC4}$, address can be changed maximum once within one page mode cycle.

## CAPACITANCE ( $T_A$=25°C, Vcc = 5V, f = 1Mz )

| DESCRIPTION | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|
| Input Capacitance (A0-A11) | $C_{IN1}$ | - | 90 | pF |
| Input Capacitance (/W) | $C_{IN2}$ | - | 122 | pF |
| Input Capacitance (/RAS0) | $C_{IN3}$ | - | 38 | pF |
| Input Capacitance (/CAS0-/CAS3) | $C_{IN4}$ | - | 38 | pF |
| Input/Output Capacitance (DQ0-31) | $C_{DQ1}$ | - | 17 | pF |

## AC CHARACTERISTICS ( 0°C ≤ $T_A$ ≤ 70°C , Vcc = 5V±10%, See notes 1,2.)

| PARAMETER | SYMBOL | -5 | | -6 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| Random read or write cycle time | $t_{RC}$ | 84 | | 104 | | ns |
| Access time from /RAS | $t_{RAC}$ | | 50 | | 60 | ns |
| Access time from /CAS | $t_{CAC}$ | | 13 | | 15 | ns |
| Access time from column address | $t_{AA}$ | | 25 | | 30 | ns |
| /CAS to output in Low-Z | $t_{CLZ}$ | 3 | | 3 | | ns |
| Output buffer turn-off delay | $t_{OFF}$ | 3 | 13 | 3 | 15 | ns |
| Transition time (rise and fall) | $t_T$ | 1 | 50 | 1 | 50 | ns |
| /RAS precharge time | $t_{RP}$ | 30 | | 40 | | ns |
| /RAS pulse width | $t_{RAS}$ | 50 | 10K | 60 | 10K | ns |
| /RAS hold time | $t_{RSH}$ | 13 | | 15 | | ns |
| /CAS hold time | $t_{CSH}$ | 38 | | 45 | | ns |
| /CAS pulse width | $t_{CAS}$ | 8 | 10K | 10 | 10K | ns |
| /RAS to /CAS delay time | $t_{RCD}$ | 20 | 37 | 20 | 45 | ns |
| /RAS to column address delay time | $t_{RAD}$ | 15 | 25 | 15 | 30 | ns |
| /CAS to /RAS precharge time | $t_{CRP}$ | 5 | | 5 | | ns |
| Row address set-up time | $t_{ASR}$ | 0 | | 0 | | ns |

| | | | | | | |
|---|---|---|---|---|---|---|
| Row address hold time | $t_{RAH}$ | 10 | | 10 | | ns |
| Column address set-up time | $t_{ASC}$ | 0 | | 0 | | ns |
| Column Address to /RAS lead time | $t_{RAL}$ | 25 | | 30 | | ns |
| Read command set-up time | $t_{RCS}$ | 0 | | 0 | | ns |
| Read command hold referenced to /CAS | $t_{RCH}$ | 0 | | 0 | | ns |
| Read command hold referenced to /RAS | $t_{RRH}$ | 0 | | 0 | | ns |
| Write command hold time | $t_{WCH}$ | 10 | | 10 | | ns |
| Write command hold referenced to /RAS | $t_{WCR}$ | 50 | | 55 | | ns |
| Write command pulse width | $t_{WP}$ | 10 | | 10 | | ns |
| Write command to /RAS lead time | $t_{RWL}$ | 13 | | 15 | | ns |
| Write command to /CAS lead time | $t_{CWL}$ | 8 | | 10 | | ns |
| Data-in set-up time | $t_{DS}$ | 0 | | 0 | | ns |
| Data-in hold time | $t_{DH}$ | 8 | | 10 | | ns |
| Refresh period | $t_{REF}$ | | 64 | | 64 | ns |
| Write command set-up time | $t_{WCS}$ | 0 | | 0 | | ns |
| /CAS setup time (C-B-R refresh) | $t_{CSR}$ | 5 | | 5 | | ns |
| /CAS hold time (C-B-R refresh) | $t_{CHR}$ | 10 | | 10 | | ns |
| /RAS precharge to /CAS hold time | $t_{RPC}$ | 5 | | 5 | | ns |

**NOTES**

1. An initial pause of 200µs is required after power-up followed by any 8 /RAS-only or /CAS-before-/RAS refresh cycles before proper device operation is achieved.
2. $V_{IH\ (min)}$ and $V_{IL\ (max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If $t_{RCD}$ is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by $t_{CAC}$.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$
6. $t_{AR}$, $t_{WCR}$, $t_{DHR}$ are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to $V_{OH}$ or $V_{OL}$.
8. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$ anf $t_{AWD}$ are non restrictive operating parameter.
   They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.
10. These parameters are referenced to the /CAS leading edge in early write cycles and to the /W leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD}$ is greater than the specified $t_{RAD(max)}$ limit. then access time is controlled by $t_{AA}$.

## AC CHARACTERISTICS ( $0\ ^{o}C \leq T_A \leq 70^{o}C$ , Vcc = 5V±10%)

| PARAMETER | SYMBOL | -5 | | -6 | | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| Hyper page mode cycle time | $t_{HPC}$ | 20 | | 25 | | ns | 11 |
| /CAS precharge time (Hyper page cycle) | $t_{CP}$ | 8 | | 10 | | ns | |
| /RAS pulse width (Hyper page cycle) | $t_{RASP}$ | 50 | 200K | 60 | 200K | ns | |
| /RAS hold time from /CAS precharge | $t_{RHCP}$ | 30 | | 35 | | ns | |
| /W to RAS precharge time (C-B-R refresh) | $t_{WRP}$ | 10 | | 10 | | ns | |
| /W to RAS hold time (C-B-R refresh) | $t_{WRH}$ | 10 | | 10 | | ns | |
| Output data hold time | $t_{DOH}$ | 5 | | 5 | | ns | |
| Output buffer turn off delay from /RAS | $t_{REZ}$ | 3 | 13 | 3 | 15 | ns | 6,12 |
| Output buffer turn off delay from W | $t_{WEZ}$ | 3 | 13 | 3 | 15 | ns | 6 |
| /W to data delay | $t_{WED}$ | 15 | | 15 | | ns | |
| /W puls width | $t_{WPE}$ | 5 | | 5 | | ns | |

**NOTES**

1. An initial pause of 200us is required after power-up followed by any 8 /RAS-only or /CAS-before-/RAS refresh cycles before proper device operation is achieved.
2. Input voltage levels are Vih/Vil. $V_{IH}$(min) and $V_{IL}$(max) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$(min) and $V_{IL}$(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the $t_{RCD}$(max) limit insures that $t_{RAC}$(max) can be met. $t_{RCD}$(max) is specified as a reference point only. If $t_{RCD}$ is greater than the specified $t_{RCD}$(max) limit, then access time is controlled exclusively by $t_{CAC}$.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit and is not referenced for $V_{OH}$ or $V_{OL}$.
7. $t_{WCS}$ is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.
9. These parameters are referenced to the /CAS leading edge in early write cycles.
10. Operation within the $t_{RAD}$(max) limit insures that $t_{RAC}$(max) can be met. $t_{RAD}$(max) is specified as reference point only. If $t_{RAD}$ is greater than the specified $t_{RAD}$(max) limit access time is controlled by $t_{AA}$.
11. tASC ≥6ns, Assume t T=2.0ns.
12. If /RAS goes high before /CAS high going, the open circuit condition of the output is achieved by /CAS high going. If /CAS goes high before /RAS high going , the open circuit condition of the output is achieved by /RAS going.

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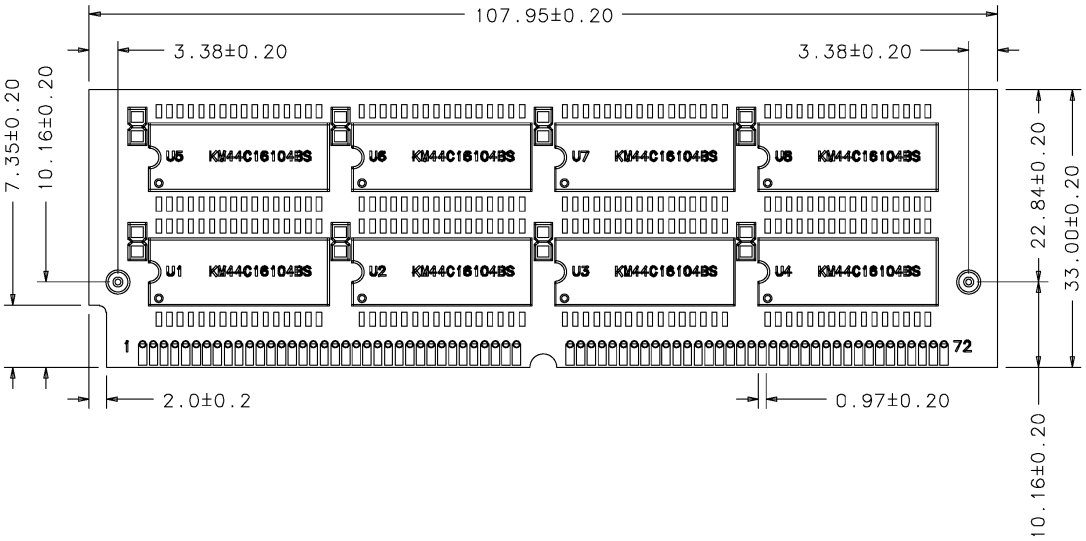
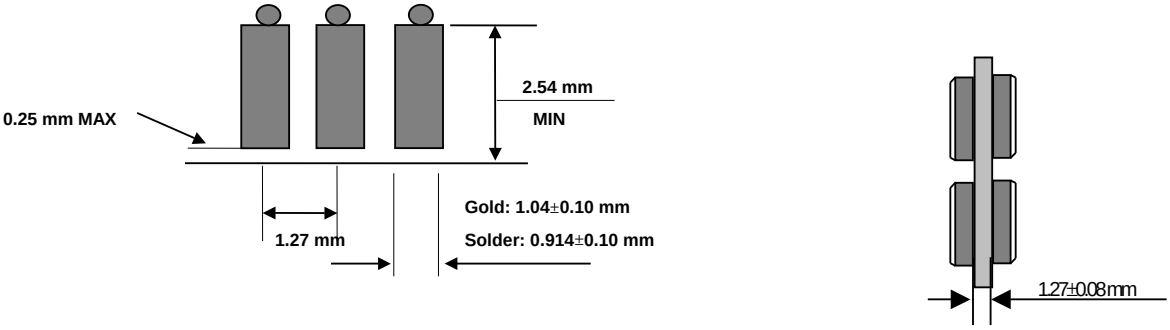
## PACKAGING INFORMATION




(Solder & Gold Plating)

## ORDERING INFORMATION

| Part Number | Density | Org. | Package | Component Number | Vcc | MODE | SPEED |
|---|---|---|---|---|---|---|---|
| **HMD32M32M16G-5** | 128Byte | x 32 | 72 Pin-SIMM | 16EA | 5V | FPM | 50ns |
| **HMD32M32M16G-6** | 128Byte | x 32 | 72 Pin-SIMM | 16EA | 5V | FPM | 60ns |